REMARKS

Objections to the Specification

The disclosure is objected to because of the informalities on line 1-5 of page 7. In particular, the Examiner objected to the recitation "the magnitude of the differential signal outputted from the output circuit 20 can be controlled through controlling the magnitude of the first voltage V1 and the second voltage V2 provided by the reference current control circuit 50" which the Examiner states is misdescriptive with respect to the operation of the circuit. Applicant respectfully submits that the Examiner's analysis is incorrect.

Referring to FIG. 5 of the specification, the gate voltages of the transistors 21, 22, 23, 24 are VDD, V2, V1, and GND, respectively. The transistors 21, 24 are OFF because the source-gate voltages V_{SG} of the transistors 21, 24 are equal to 0 (V_{SG} = (VDD-VDD) or (GND-GND)), ***the drain current I_D of the transistor 23 is generated according to the source-gate voltage V_{SG} of the transistor 23 (V_{SG} = VDD-V1), and the drain current I_D of the transistor 22 is generated according to the source-gate voltage V_{SG} of the transistor 23 (V_{SG} = GND-V2)***. The magnitude of the differential signal is equal to $I_D \times R_L$ and the drain current I_D of the second and the third transistors 22, 23 are generated according to the control voltages (V1,V2).

Referring now to FIG. 6 of the specification, ***the drain current I_D of the first transistor 21 is generated according to the source-gate voltage V_{SG} of the first transistor 21 (V_{SG} = VDD-V1), and the drain current I_D of the fourth transistor 24 is generated according to the source-gate voltage V_{SG} of the fourth transistor 24 (V_{SG} = GND-V2)***. The magnitude of the differential signal is equal to $I_D \times R_L$ and the drain current I_D of the first and the fourth transistors 21,24 are generated according to the control voltages (V1,V2).

Thus, it follows from the above that the magnitude ($I_D \times R_L$) of the differential signal outputted from the output circuit 20 can be controlled through controlling the

magnitude of the control voltages (V1,V2) provided by the reference current control circuit.

The Examiner further states that "the control voltages (V1-V2) controlling the on/off of the transistors (21-24) of the output circuit so the control voltages (V1, V2) only control the phase (i.e., pulse width) of the differential signal (LVDS+, LVDS-)". Applicant respectfully submits that the Examiner's analysis is incorrect.

When the first switching signal S1 is HIGH and the second switching signal S2 is LOW, the gate voltages of the first, the second, the third, and the fourth transistors 21, 22, 23, and 24 are VDD, V2, V1, and GND, respectively, and the differential signal is "High" (i.e., $V_{LVDS+, LVDS-} = I_{REF}R_L$).

When the first switching signal S1 is LOW and the second switching signal S2 is HIGH, the gate voltages of the first, the second, the third, and the fourth transistors 21, 22, 23, and 24 are V1, GND, VDD, and V2, respectively, and the differential signal is "LOW" (i.e., $V_{LVDS+, LVDS-} = - I_{REF}R_L$).

The gate voltages of the first, the second, the third, and the fourth transistors 21, 22, 23, and 24 are controlled by the first and the second switching signal (S1, S2) outputted from the switch control circuit 40. Thus, it is the first and the second switching signals (S1, S2) that control the phase (i.e., pulse width) of the differential signal.

As to the Examiner's statement that "the magnitude of the differential signal is determined based on the power supply VDD of the circuit (i.e., the magnitude of the differential signal (LVDS+, LVDS-) is VDD.)", Applicant respectfully submits that the Examiner's analysis is incorrect.

Referring to the specification (at page 6, line 9-15), $VDD > I_{REF}R_L+\Delta V_{23}+\Delta V_{22}$, wherein VDD is an operational voltage source (i.e., power supply); $I_{REF}R_L$ is the magnitude of the differential signal; I_{REF} represents the drain current I_D of the first and the fourth transistors or the second and the third transistors; and ΔV_{23} and ΔV_{22} are the drain-to-source voltage drops of the transistors 23 (or 21) and 22 (or 24) respectively. Accordingly, ***the magnitude ($I_{REF}R_L$) of the differential signal (LVDS+, LVDS-) must be smaller than the VDD.***

For at least these reasons, withdrawal of this objection is respectfully requested.

Objection to Claims 1-17 for Informalities

Claims 1-17 are objected to due to informalities. Claims 1, 2, and 14 have been amended substantially in accord with the Examiner's suggestions. Accordingly, withdrawal of this objection is respectfully requested.

Rejection of claims 1-17 under 35 U.S.C. § 112, Second Paragraph

Claims 1-17 currently stand rejected as being indefinite. This rejection is respectfully traversed for the following reasons.

Regarding the rejection of claim 1, the Examiner states that the recitation "the magnitude of the differential signal is determined based on the control voltage" is indefinite because it is inconsistent with the operation of the circuit. The operation of the circuit has been addressed in detail above, in the section titled "Objections to the Specification". Applicant respectfully submits that for the reasons cited above, the operation of the circuit is consistent with the language recited in claim 1.

Regarding the rejection of claim 6, Applicant has amended claim 6 to incorporate the Examiner's suggested language.

Regarding the rejection of claim 11, Applicant has amended claim 11 to recite "the second, the third, the fifth, and the eighth switches" and "the first, the fourth, the sixth, and the seventh switches" instead of transistors.

Regarding the rejection of claim 12, Applicant has amended claim 12 to improve the clarity of the language and has eliminated the indefinite use of "it".

It is respectfully submitted that the amendments to the claims, along with amendments to the specification, overcome the rejections under 35 U.S.C. § 112, second paragraph. Accordingly, withdrawal of this rejection is respectfully requested.

Rejection of claims 1-8 and 10-17 under 35 U.S.C. § 102(e)

Claims 1-8 and 10-17 currently stand rejected as anticipated by the Lye patent (U.S. patent 6,566,933). This rejection is respectfully traversed for the following reasons.

Regarding claim 1, the Examiner states that Fig.3 of the Lye patent shows, *inter alia*, "a reference current control circuit (I1, I2, [...]) to provide a control voltage (VDD, VSS) to the output circuit such that ***the magnitude of the differential signal is determined based on the control voltage***" (emphasis added). However, Lye fails to teach or suggest that the currents I1 and I2 are determined by the VDD or GND or the voltage (VMID), and Lye fails to disclose that the outputs from the differential pairs 70 and 72 are determined based on the VDD or GND or the voltage (VMID).

According to the detailed description of the Lye patent, "two MOS devices 12 and 14 with their sources connected together (a differential pair), together with a current source 16 supplying current I_0 to the common source node of the differential pair. When the gate 20 of the MOS 12 is driven to a high voltage and the gate 22 of the MOS 14 is driven to a low voltage, any circuitry at the drain 24 of the MOS 12 will see $I_1=I_0$, while any circuitry at the drain 28 of the MOS 14 will see I2=0. ..., then at drain 24, I1=0 and at drain 28, $I_2=I_0$" (Col. 1, lines. 22-34), and "the system is susceptible to distortion in the output waveforms I_1 and I_2" (Col. 1, lines. 46-47). Thus, it is shown that the output waveforms I_1 and I_2 of the differential pair are dependent on the current source 16 supplying current I_0.

Further, according to Lye, "the driver circuit 64 comprises MOS devices M1, M2, M3 and M4 and current source I1 and I2 connected to MOS devices M1 and M2, and M3 and M4 respectively." (Col. 4, ll. 21-24), and "the outputs from the differential pairs 70 and 72 form a Class AB (current source/sink) output pair that may be driven off-chip through resistors to form a voltage" (Col. 4, ll. 43-45). Lye fails to disclose that the currents I1 and I2 are determined by VDD, GND, or VMID, and thus it follows that Lye fails to disclose that the outputs from the differential pairs 70 and 72 are determined based on the VDD or GND or the voltage (VMID).

Because Lye fails to disclose all of the elements of claim 1, the rejection is inappropriate and withdrawal of the rejection is respectfully requested. Regarding the rejections of claims 2-8 and 10-17, which all depend from claim 1, withdrawal of the rejections of the dependent claims is respectfully requested for the reasons cited for claim 1.

General Comments

Applicant has added new claims 18-23. Claim 18 is a new dependant claim depending from claim 1. Claim 19 is a new independent claim, reciting that a first and a second transistor are directly coupled to an operational voltage source, or a third and a fourth transistors are directly coupled to ground or both. Such an arrangement is not taught by Lye. Thus, Applicant respectfully submits that claim 19, and new dependant claims 20-23, are allowable over the cited reference.

Conclusion

In view of the amendments to the claims, and in further view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is requested that claims 1-23 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's attorney, the Examiner is invited to contact the undersigned at the numbers shown.

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